SPECIFICATION
FOR
EPD Module

MODULE No:	KD027QVFSN007
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2023.06.25	V1.0	ALL	FIRST ISSUE

Contents

1. Over View

KD027QVFSN007 is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The 2.6” active area contains 152x296 pixels. The module is a TFT- array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

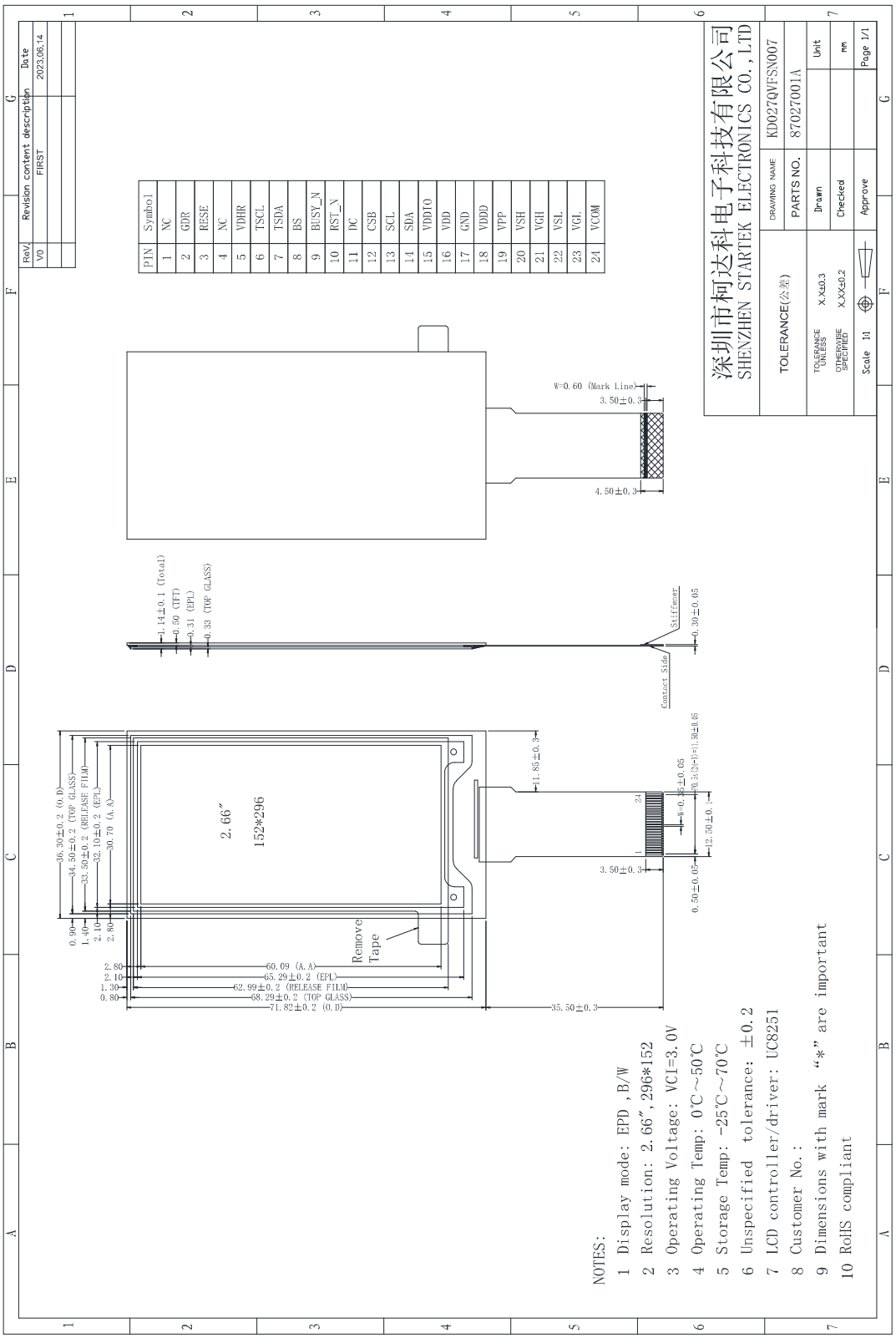
2. Features

- 296×152 pixels display
- White reflectance above 30%
- Contrast ratio above 8:1
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Landscape, portrait modes
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I²C signal master interface to read external temperature sensor

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.6	Inch	
Display Resolution	152(H) x 296(V)	Pixel	
Active Area	30.7(H) x 60.09(V)	mm	
Pixel pitch	0.202(H) x 0.203(V)	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.3(H) x 71.82(V) x 1.14(D)	mm	
Module Weight	6	g	
Controller IC	UC8251		
Interface	3Wire / 4Wire SPI	-	
Display mode	EPD,B / W	-	
Operating temperature	0～+50	℃	
Storage temperature	-25～+70	℃	

4. Mechanical Drawing of EPD module



PIN	Symbol
1	NC
2	GDR
3	RESE
4	NC
5	VDHR
6	TSCL
7	TSDA
8	BS
9	BUSY_N
10	RST_N
11	DC
12	CSB
13	SCL
14	SDA
15	VDDIO
16	VDD
17	GND
18	VDDD
19	VPP
20	VSH
21	VGH
22	VSL
23	VGL
24	VCOM

5. Input/Output Pin Assignment

NO.	Name	DISCRIPTION	I/O	Remark
1	NC	NO Connection	-	Keep open
2	GDR	N-Channel MOSFET Gate Drive Control	O	
3	RESE	Current Sense Input for the Control Loop	I	
4	NC	NO Connection	-	Keep open
5	VDHR	Positive Source driving voltage	C	
6	TSCL	IIC Interface to digital temperature sensor Clock pin	O	
7	TSDA	IIC Interface to digital temperature sensor Data pin	I/O	
8	BS	Bus Interface selection pin	I	Note 5-4
9	BUSYN	Busy state output pin	O	Note 5-3
10	RSTN	Reset signal input. Active Low.	I	
11	D/C	Data /Command control pin	I	Note 5-2
12	CSB	Chip select input pin	I	Note 5-1
13	SCL	Serial Clock pin (SPI)	I	
14	SDA	Serial Data pin (SPI)	I/O	
15	VDD	Power Supply for interface logic pins It should be connected with VCI	P	
16	VDD	Power Supply for the chip	P	
17	VSS	Ground	P	
18	VDDD	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	C	
19	VPP	FOR TEST	P	
20	VSH	Positive Source driving voltage	C	
21	VGH	Positive Gate driving voltage	C	
22	VSL	Negative Source driving voltage	C	
23	VGL	Negative Gate driving voltage	C	
24	VCOM	VCOM driving voltage	C	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output),
P = Power Pin, C =Capacitor Pin

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode.
When the pin is pulled HIGH, the data at D1 will be interpreted as data.
When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin Low when
- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensorNote

5-4: Bus interface selection pin

BS State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{dd}	-0.5 to +4.0	V
Logic Input voltage	V_{IN}	-0.5 to V_{dd}+0.5	V
Logic Output voltage	V_{OUT}	-0.5 to V_{dd}+0.5	V

Note: Maximum ratings are those values beyond which damages to the device may occur.
Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VDD=3.0V, T_{OPR} =25ºC

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{dd}	-	VDD	2.4	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.8 V_{dd}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2V_{dd}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{dd}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1V_{dd}	V
OTP Program voltage	V_{pp}	-	V_{pp}	-	8.25	-	V
Typical power	P_{TYP}	-	-	-	12	120	mW
Deep sleep mode	P_{STPY}	-	-	-	4.0	-	mW
Typical operating current	Iopr_V_{CI}	V_{dd} =3.0V	-	-	4.0	10	mA
Sleep mode current	Islp_VDD	DC/DC off No clock No input load Ram data retain	VDD	-	26	-	uA
Deep sleep mode current	Idslp_VDD	DC/DC off No clock No input load Ram data not retain	VDD	-	1	-	uA

Notes:1.The typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.

2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by SID.

6.3 AC Characteristics

6.3.1 MCU Interface selection

The pin assignment at different interface mode is summarized in Table.Different MCU mode can be set by hardware selection on BS pins.The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CSB	D/C	RSTN
BS=L 4-wire SPI	SDIN	SCLK	CSB	D/C	RSTN
BS=H 3-wire SPI	SDIN	SCLK	CSB	L	RSTN

6.3.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

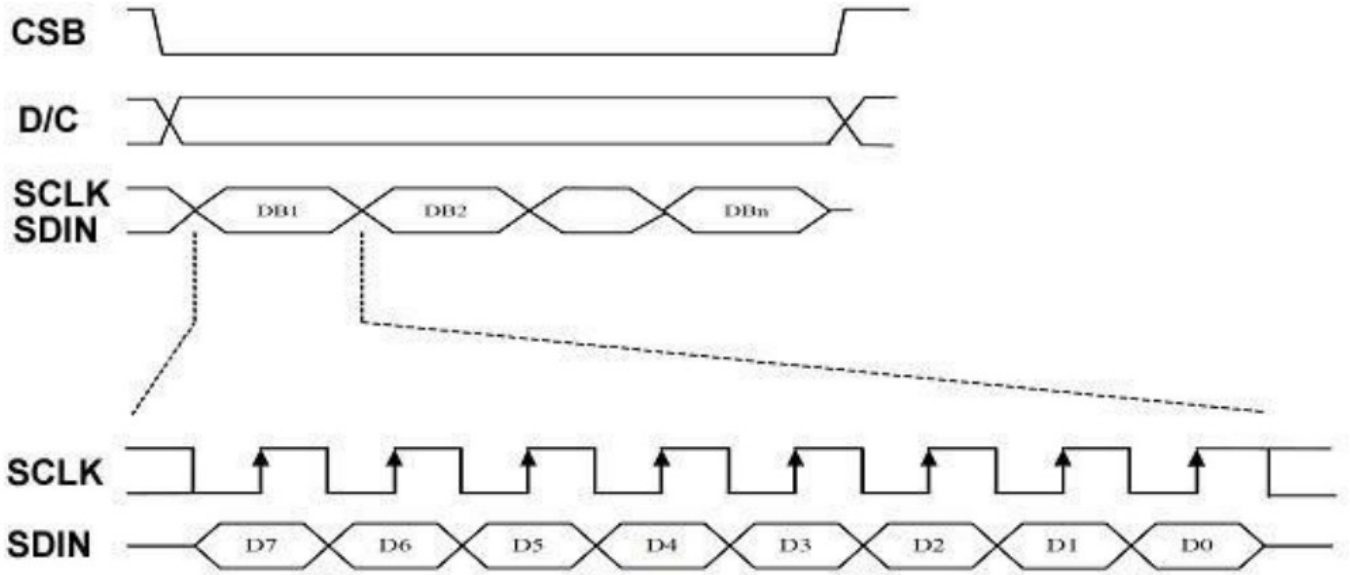
Function	CSB	D/C	SCLK
Write command	L	L	↑
Write data	L	H	↑

Note:

(1) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.



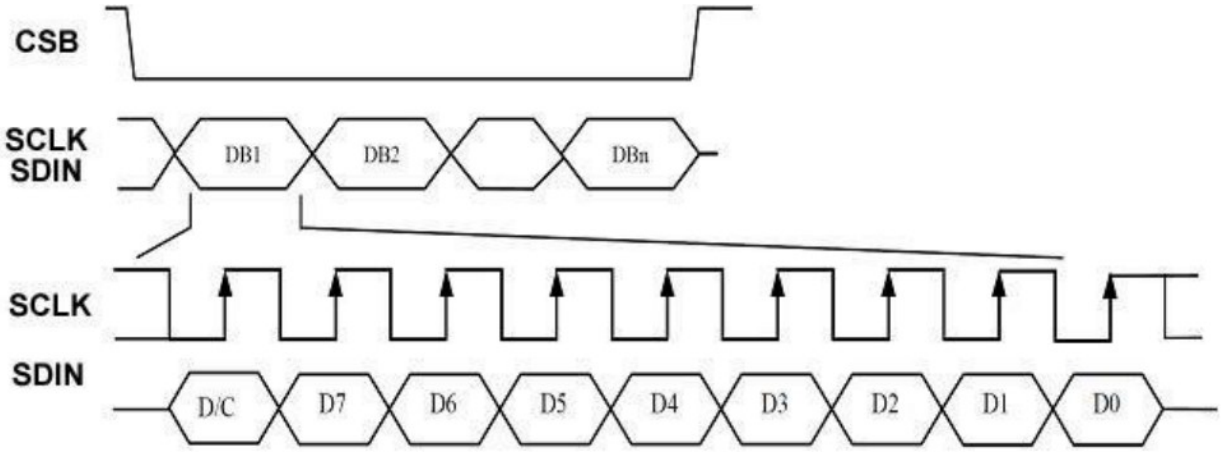
Write procedure in 4-wire SPI mode

6.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN. The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C bit = 1) or the command register (D/C bit = 0).

Function	CSB	D/C	SCLK
Write command	L	Tie	↑
Write data	L	Tie	↑

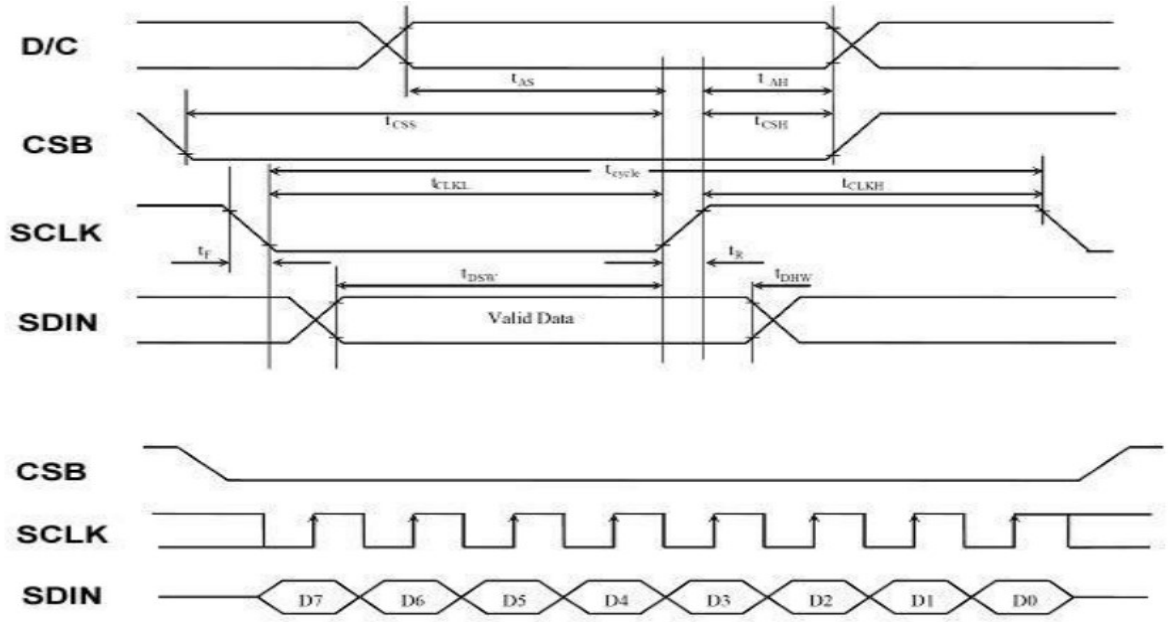
Note: ↑ stands for rising edge of signal



Write procedure in 3-wire SPI mode

6.3.4 Interface Timing

The following specifications apply for: VSS=0V, VDD=3.0V, TOPR=25ºC



(V_{dd} - VSS = 2.4V to 3.3V, T_{OPR} = 25°C, CL=20pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~80%]	-	-	15	ns

7. Optical Characteristics

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Values				
			Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	7-1
CR	Contrast Ratio		8:1	10:1	-	-	7-2
White △L 24h	Reduce	-		≤4	-	-	-
T_{update}	Image update time	at 25 °C	-	2800	-	ms	-

Notes: 7-1. Luminance meter: Eye-One Pro Spectrophotometer.

7-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

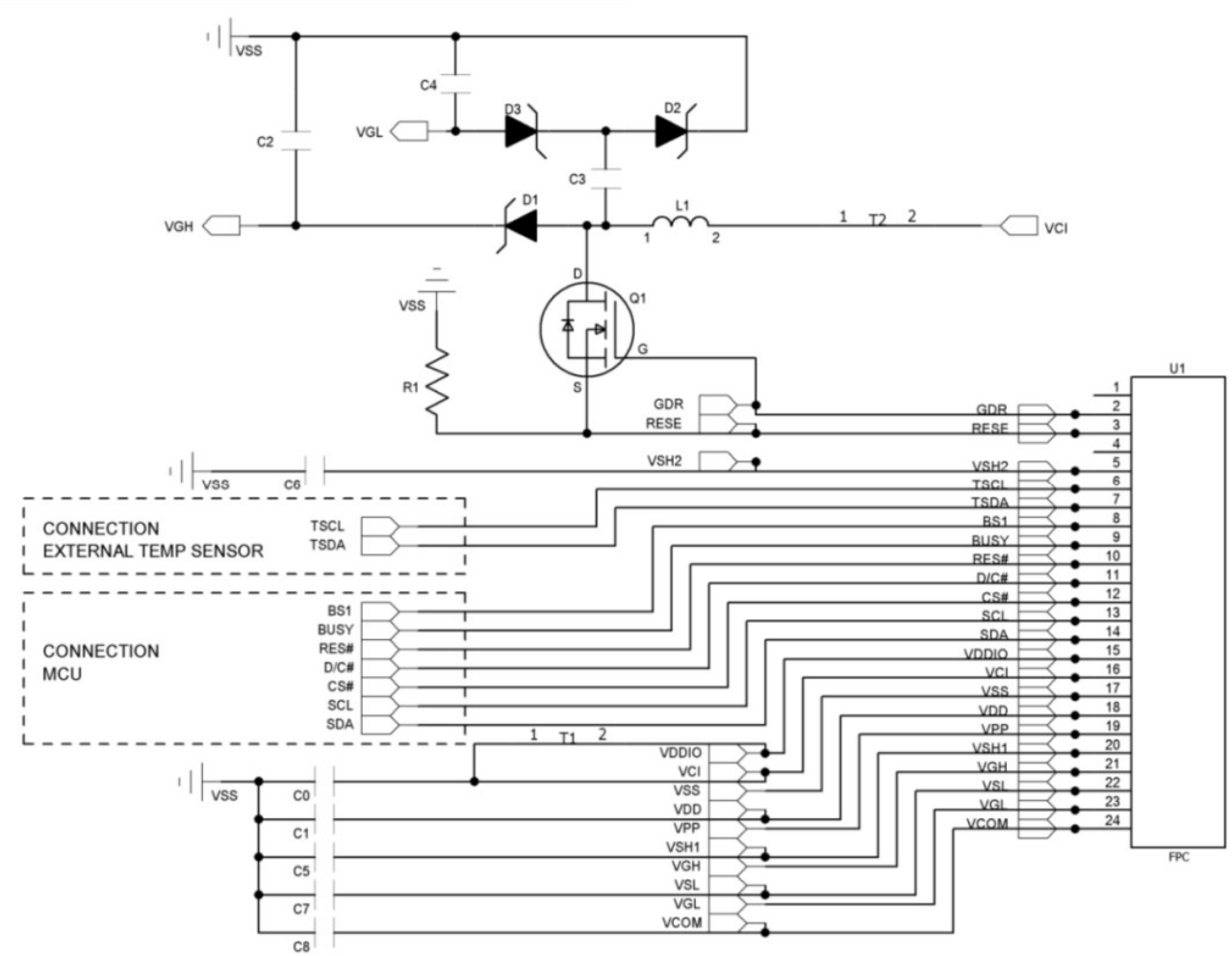
8. Handling, Safety and Environment Requirements

1. The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel .
2. The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
3. Do not apply pressure to the EPD panel in order to prevent damaging it .
4. Do not connect or disconnect the interface connector while the EPD panel is in operation
5. Do not stack the EPD panels / Modules.
6. Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.
7. Do not disassemble or reassemble the EPD panel .
8. Use a soft dry cloth without chemicals for cleaning. Please don’t press hard for cleaning because t he surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet.
9. Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation .
10. It’s low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.
11. High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package. Without sunlight, without condensation a temperature range of 15° C to 35° C, and humidity from 30%RH to 60%RH.

9. Reliability test

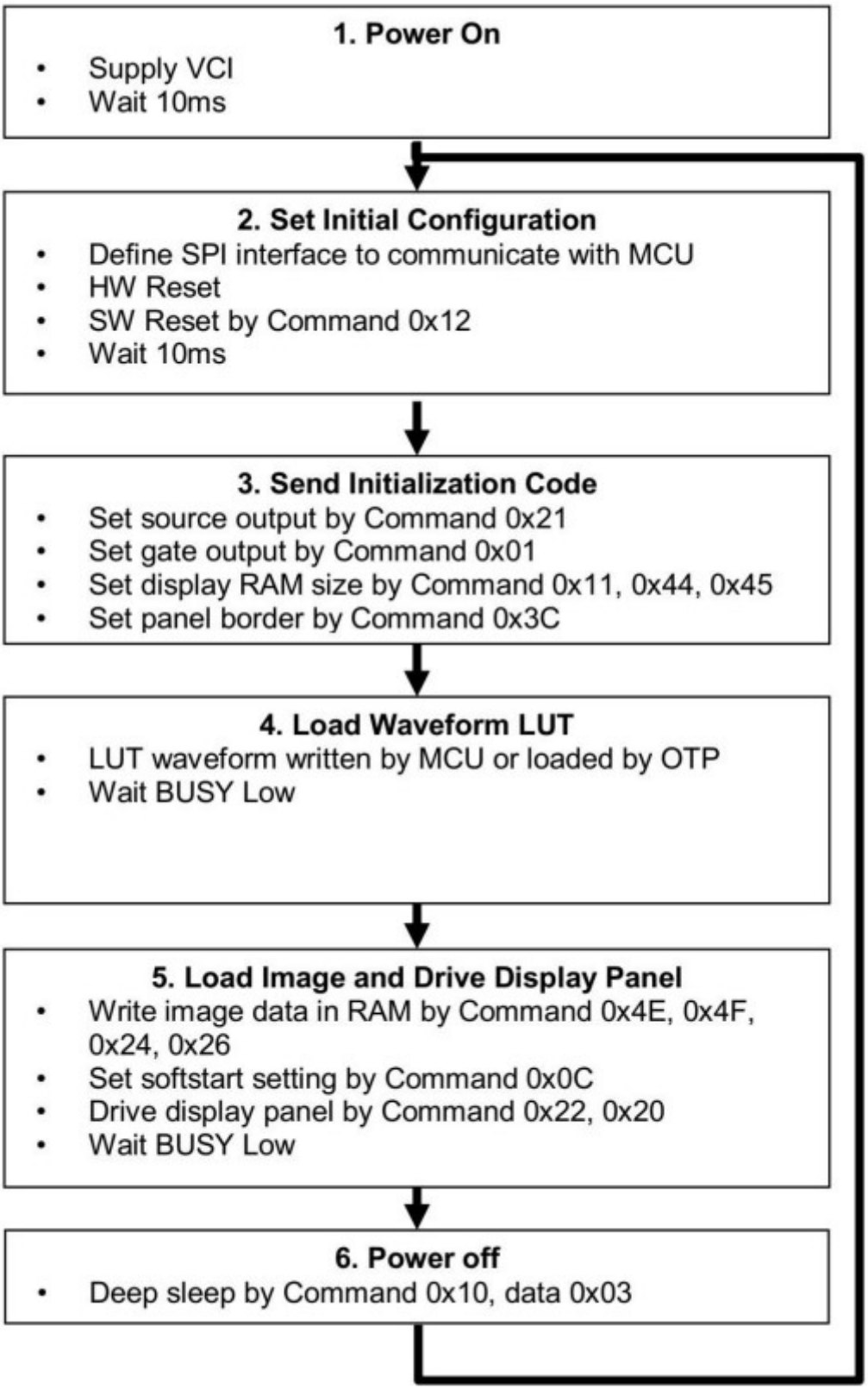
NO.	Test items	Test condition	Method	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
4	Low-Temperature Storage	T = -25°C for 240 hrs	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High-Temperature High-Humidity Operation	T = +40°C, RH = 90% For 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
6	High Temperature High Humidity Storage	T = +60°C, RH=80% For 240hrs	IEC 60 068-2-3CA	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
7	Thermal Shock	1cycle:[-25°C 30min]→ [+70°C 30min]: 100cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full Packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence:1 corner, 3edges, 6 faces One drop for each	Full Packed for shipment	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.

10. Typical Application Circuit with SPI Interface



Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
R1	2.2 ohm	0402/0603/0805; 1% variation, ≥ 0.05W
D1-D3	Diode	MBR0530 1) Reverse DC voltage ≥ 30V 2) Io ≥ 500mA 3) Forward voltage ≤ 430mV
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≥ 30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47uH	CDRH2D18 / LDNP-470NC Io= 500mA (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

11. Typical Operating Sequence



12. Inspection condition

12.1 Environment

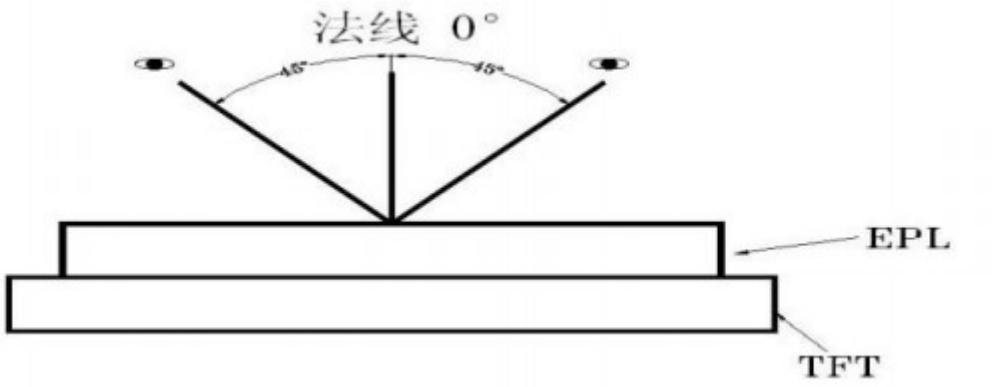
Temperature： 25±3 ℃

Humidity：55±10%RH

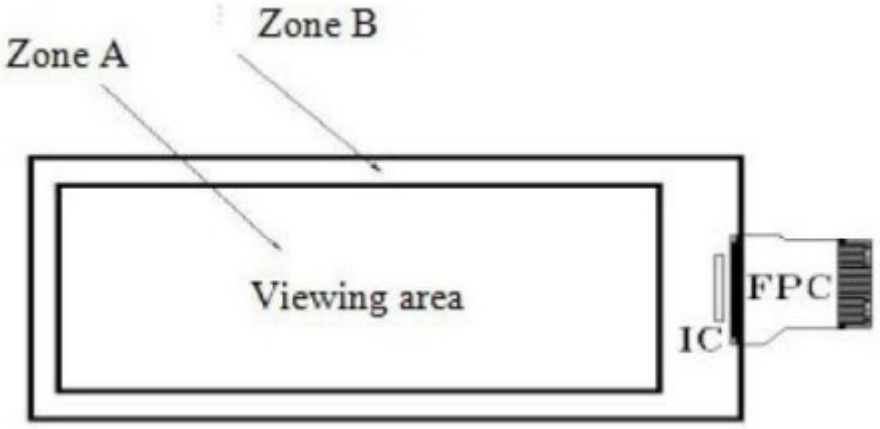
12.2 Illuminance

Brightness:1200～1500LUX; distance: 30CM; Angle: Relate 45°surround.

12.3 Inspect method

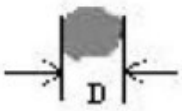
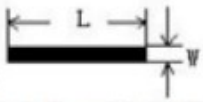


12.4 Display area

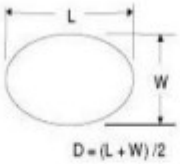
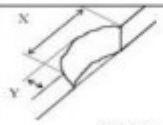
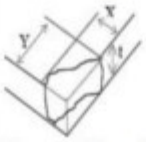
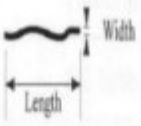


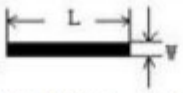
12.5 Inspection standard

12.5.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.3mm，Allowed 0.3mm＜D≤0.5mm。N≤3， 0.5mm＜D Not Allow	MI		
3	Black/White spots (No switch)	 L≤1.0mm,W≤0.15mm negligible 1.0mm＜L≤4.0mm 0.15mm＜W≤0.5mm N≤4 allowable L＞4.0mm ,W＞0.5mm is not allowed		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			

12.5.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.3mm，Allowed 0.3mm＜D≤0.5mm，N≤5 D＞0.5mm，Not Allow	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	\Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm  2mm≤X or 2mm≤Y Allow  W≤0.1mm,L≤5mm, n≤ 2 Edge crown：X≤0.3mm，Y≤3mm	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	  Not Allow	MA	Visual / Microscope	Zone B

8	B/W Line	 L≤1.0mm,W≤0.15mm negligible 1.0mm<L≤4.0mm 0.15mm<W≤0.5mm N≤4 allowable L>4.0mm ,W>0.5mm is not allowed	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	TFT edge bulge: X≤3mm，Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	D≤0.25mm, allow 0.25mm<D≤0.4mm ,n≤4 allow D>0.4mm is not allowed (n≤8 items are allowed within 5 mm in diameter)	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives seep in≤1/2 Margin width Length excluding Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤0.5mm。n≤5	MI		
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	Zone B
14	Silicon glue	Thickness ≤ PS surface(With protect film): Full cover the IC; Shape: The width on the FPC ≤ 0.5mm (Front) The width on the FPC≤1.0mm (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 t≤1.5mm	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

13. Packaging